Maratha Vidya Prasarak Samaj's

Karmaveer Adv. Baburao Ganpatrao Thakare College of Engineering

An Autonomous Institute affiliated to Savitribai Phule Pune University, Pune

Udoji Maratha Boarding Campus, Gangapur Road, Nashik - 422 013, Maharashtra, India

Post-Gratuate Program Syllabus

First Year M.Tech. Electronics & Telecommunication Engineering (VLSI and Embedded System) (2024 Pattern)

As per NEP 2020

Academic Year 2025-26

(Copy for Student Circulation Only)

First Year M.Tech. Electronics & Telecommunication Engineering (VLSI and Embedded System)
Curriculum Structure (2024 Pattern)
Semester - I

Course Code	Course Type	Course Name	Teaching Scheme (Hrs/Week)			Evaluation Scheme and Marks						Credits			
			TH	PR	TU	CCE	ESE	TW	PR	OR	TOT	TH	PR	TU	TOT
204101	**PCC-1**	Digital CMOS Design	3	2	-	50	50	25	-	25	**150**	3	1	-	**4**
204102	**PCC-2**	Digital System Design	3	-	-	50	50	-	-	-	**100**	3	-	-	**3**
204103	**PCC-3**	Embedded System Design	3	2	-	50	50	-	25	-	**125**	3	1	-	**4**
201104	**MLC**	Research Methodologies and IPR@	4	-	-	50	50	-	-	-	**100**	4	-	-	**4**
204105X	**PEC-I**	Elective-I*	4	-	-	50	50	-	-	-	**100**	4	-	-	**4**
204106	**VSEC- I**	Skill Development Laboratory – I	-	2	-	-	-	25	-	-	**25**	-	1	-	**1**
Total			**17**	**06**	**-**	**250**	**250**	**50**	**25**	**25**	**600**	**17**	**03**	**-**	**20**

Abbreviations: **TH:** Theory **PR:** Practical **TU:** Tutorial **CCE:** Continuous Concrete Evaluation
ESE: End-Semester Examination **TW:** Term Work **OR:** Oral **TOT:** Total

@ common to all branches

First Year M.Tech. Electronics & Telecommunication Engineering (VLSI and Embedded System)
Curriculum Structure (2024 Pattern)
Semester - II

Course Code	Course Type	Course Name	Teaching Scheme (Hrs/Week)			Evaluation Scheme and Marks						Credits			
			TH	PR	TU	CCE	ESE	TW	PR	OR	TOT	TH	PR	TU	TOT
204201	**PCC-4**	Analog CMOS Design	3	2	-	50	50	25	-	25	**150**	3	1	-	**4**
204202	**PCC-5**	Devices Modeling for VLSI	4	-	-	50	50	-	-	-	**100**	4	-	-	**4**
204203	**PCC-6**	Real Time Operating System	4	2	-	50	50	25	-	-	**125**	4	1	-	**5**
204204X	**PEC-II**	Elective-II**	4	-	-	50	50	-	-	-	**100**	4	-	-	**4**
204205	**VSEC- II**	Skill Development Laboratory – II	-	2	-	-	-	25	-	-	**25**	-	1	-	**1**
204206	**ELC -I**	Seminar	-	4	-	-	-	50	-	50	**100**	-	2	-	**2**
Total			**15**	**10**	**-**	**200**	**200**	**125**	**-**	**75**	**600**	**15**	**05**	**-**	**20**

Abbreviations: **TH:** Theory **PR:** Practical **TU:** Tutorial **CCE:** Continuous Concrete Evaluation
ESE: End-Semester Examination **TW:** Term Work **OR:** Oral **TOT:** Total

Second Year M.Tech. Electronics & Telecommunication Engineering (VLSI and Embedded System)
Curriculum Structure (2024 Pattern)
Semester - III

Course Code	Course Type	Course Name	Teaching Scheme (Hrs/Week)			Evaluation Scheme and Marks						Credits			
			TH	PR	TU	CCE	ESE	TW	PR	OR	TOT	TH	PR	TU	TOT
204301	**SBC-I**	Dissertation Phase -I	-	20	-	-	-	100	-	100	**200**	-	10	-	**10**
204302	**ELC-II**	Research Seminar	-	8	-	-	-	50	-	50	**100**	-	4	-	**4**
204303	**SLC**	MOOC Courses	-	4	-	-	-	50	-	-	**50**	-	2	-	**2**
204304	**OJT**	Internship / On-Job Training	-	8	-	-	-	100	-	50	**150**	-	4	-	**4**
Total			**-**	**40**	**-**	**-**	**-**	**300**	**-**	**200**	**500**	**-**	**20**	**-**	**20**

Abbreviations: **TH:** Theory **PR:** Practical **TU:** Tutorial **CCE:** Continuous Concrete Evaluation
ESE: End-Semester Examination **TW:** Term Work **OR:** Oral **TOT:** Total

Second Year M.Tech. Electronics & Telecommunication Engineering (VLSI and Embedded System)
Curriculum Structure (2024 Pattern)
Semester - IV

Course Code	Course Type	Course Name	Teaching Scheme (Hrs/Week)			Evaluation Scheme and Marks						Credits			
			TH	PR	TU	CCE	ESE	TW	PR	OR	TOT	TH	PR	TU	TOT
204401	**SBC-II**	Dissertation Phase -II	-	40	-	-	-	200	-	100	**300**	-	20	-	**20**
Total			**-**	**40**	**-**	**-**	**-**	**200**	**-**	**100**	**300**	**-**	**20**	**-**	**20**

Abbreviations: **TH:** Theory **PR:** Practical **TU:** Tutorial **CCE:** Continuous Concrete Evaluation
ESE: End-Semester Examination **TW:** Term Work **OR:** Oral **TOT:** Total

Program Elective Course - I and II

Course Code	* Elective -I	Course Code	** Elective -II
204105A	Micro & Nano Electro Mechanical Systems (MEMS & NEMS)	204204A	System on Chip Design
204105B	ASIC Design	204204B	VLSI Testing & Testability
204105C	Embedded Automotive System	204204C	Embedded system for Biomedical
204105D	Electromagnetic Interference and Compatibility in ESD	204204D	Security in Embedded System

List of Abbreviations Used with Percentage of Credits

Abbreviations	Course Type	Number of Courses	Credits	% of Credits
PCC	Program Core Course	06	21	25.0
PEC	Program Elective Course	02	08	10.0
PLC	Program Laboratory Course	04	04	5.0
ELC	Experiential Learning Course	02	06	7.5
MLC	Mandatory Learning Course	01	04	5.0
VSEC	Vocational and Skill Enhancement Course	02	02	2.5
SBC	Skill Based Course	02	30	37.5
SLC	Self-Learning Course	02	06	7.5
Total		21	80	100%

- **Summary of Credits and Total Marks:**

Semester	Credits	Marks
I	20	600
II	20	600
III	20	500
IV	20	300
Total	**80**	**2000**

• Definition of Credit :

The Post Graduate (P.G.) programmes will have credit system. The details of credit will be as follow.

1 Credit = 1 hour/week for lecture
= 2 hours/week for practical
= 1 hour/week for tutorial

Semester - I

Course Code: 204101	Course Name: Digital CMOS Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 3 Hours/Week **Practical :** 2 Hours/Week	**3** **1**	**CCE :** 50 Marks **ESE :** 50 Marks **TW :** 25 Marks **OR :** 25 Marks

Prerequisite Courses:

- Basics of Digital circuits.

Course Objectives:

- To learn MOSFET Models and layout fundamentals.
- To nurture students' understanding in performance parameters of digital CMOS Design.
- To understand the advanced trends in CMOS design.
- To learn the delay models.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand the fundamentals of CMOS Technology in Digital Domain.

CO2: Analyze and design combinational and sequential logic circuits using CMOS technology.

CO3: Evaluate performance metrics such as delay, power consumption and area in CMOS circuits.

CO4: Apply design rules and layout techniques for CMOS-based VLSI circuits.

CO5: Demonstrate the ability of using EDA tools in IC Design.

Course Contents

UNIT-I: MOSFET Models and Layout **09 Hours**

MOS capacitance models, MOS gate capacitance Model, MOS diffusion capacitance model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams.

UNIT-II: Performance Parameters **09 Hours**

Statistical Analysis: Introduction, Sources of error and uncertainty, One-Dimensional Static,

dynamic and short circuit power dissipations, Propagation delay, Power delay product, Fan in, fan out and dependencies. Delay Estimation: RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin.

UNIT-III: Logic Design **09 Hours**

Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tri-states, Multiplexers, Latches and Flip- Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, case study; HDL codes for FSM, Meta-stability and solutions; Transmission gate, utility and limitations.

UNIT-IV: Fault Diagnosis and Test Ability Algorithms **07 Hours**

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test.

UNIT-V: Advanced Trends **08 Hours**

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Domino logic, NORA logic, Differential Circuits, Sense Amplifier Circuits, Bi-CMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, High speed designs.

Learning Resources:

Text Books:

1. Neil Weste and Kamaran, “Principles of CMOS VLSI Design”, Education Asia
2. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson (Low Price Edition)
3. Charls Roth,“Digital System Design using VHDL”, Tata McGraw Hill.
4. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Third Edition, McGraw-Hill.
5. Samir Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, PHI.

Reference Books:

1. CMOS VLSI Design by Neil HE Weste.

Web link for MOOC / NPTEL Links:

1. https://archive.nptel.ac.in/courses/105/104/105104161/
2. https://archive.nptel.ac.in/courses/105/103/105103093/

List of Experiments / Assignments

1. To design, prepare layout and simulate CMOS Inverter, CMOS NAND, CMOS NOR for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc.
2. To design logic for ATM machine password and access functionality. Assume suitable I/Os such as card sense, 4-digit PIN number, type of account, amount, other facilities needed etc.
3. To design CMOS logic for F = A + B (C + D) + EFG and prepare layout. Assume suitable capacitive load & foundry. Measure TR, TF& TPD.
4. To draw FSM diagrams, write HDL code, synthesize, simulate, place & route for a Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. You may assume additional I/Os too.
5. To design and simulate combinational logic to demonstrate hazards. Also, simulate the same logic redesigned for removal of hazards.

Course Code: 204102	Course Name: Digital System Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 3 Hours/Week	**3**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Digital Electronics, VLSI.

Course Objectives:

- Apply the Fundamental of Digital Electronics to prepare counters.
- Analyze digital system modelling.
- Develop digital design using Programmable Logic Devices.
- Digital design development in Verilog with preparation of Testbench.
- Develop an application using Xilinx FPGA.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Design Synchronous and asynchronous counter.

CO2: Analyze controller behavior using Hardware-Software Co-design.

CO3: Implement Digital Design using Programmable Logic Devices.

CO4: Model digital design in Verilog and prepare a test bench.

CO5: Develop digital design application on Xilinx FPGA.

Course Contents:

UNIT-I: Sequential Logic Design **10 Hours**

Introduction, Moore, Mealy and Mixed type Synchronous State Machines.

Synchronous Counter Design, Hazards, Duality of sequential circuits, Different methods of minimization.

Asynchronous Counter Design, type of delays, Cycles and races, Excitation Map, Hazards, Essential hazards. Algorithmic State Machine, ASM charts, Design Procedure for ASMs. Fault Diagnosis in Sequential Circuits.

UNIT-II: Digital System Design **09 Hours**

SoC, IP Design, SoPC. Design methodology, System Modelling, Hardware- Software Co-design. Device Technology, Application Domains, Data Path, Control Path, Controller behavior and Design.

UNIT-III: Programmable Logic Devices **09 Hours**

PALs, PLDs, CPLDs and FPGAs. ASICs – Full custom, gate array based, standard cell based and Programmable ASICs, Antifuse, SRAM, EEPROM/ EPROM Technologies for Programmable ASICs.

UNIT-IV: Verilog for Synthesis **09 Hours**

Introduction, Behavioral, Data flow, Structural Models, Simulation Cycles, Process Concurrent Statements Sequential Statements Loops Delay Models Sequential Circuits, FSM Coding, Library, Packages, Functions, Procedures, Operator Inferencing, Test bench.

UNIT-V: Xilinx FPGA **08 Hours**

Introduction Logic Block Architecture, Routing Architecture, Programmable Interconnections, Design Flow, Xilinx Artix 7 (Architecture), Altera Stratix, Actel 54SX Architecture, Boundary Scan, Programming FPGA's, Constraint Editor, Static Timing Analysis, One hot encoding, Applications, Tools.

Case Studies:

1. Xilinx Virtex II Pro: Embedded System on Programmable Chip,
2. Hardware-software co-simulation, Bus function models, BFM Simulation,
3. Debugging FPGA Design, Chipscope Pro.

Learning Resources:

Text Books:

1. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.
2. Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, Second Edition, 2011.
3. David Greaves, “Modern System-on-Chip Design” Arm , 2021.
4. Taub and Schilling, “Digital Principles and Applications” TMH.

Reference Books:

1. Wayne Wolf, FPGA Based System Design, Prentices Hall Modern Semiconductor Design Series, 2011
2. S,Brown and Z,Vranesic, “Fundamentals of Digital Logic with Verilog Design”, Tata Mc Graw Hill, 2008.

Weblink for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/117108040

Course Code: 204103	Course Name: Embedded System Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 3 Hours/Week **Practical** : 2 Hours/Week	**3** **1**	**CCE** : 50 Marks **ESE** : 50 Marks **PR** : 25 Marks

Prerequisite Courses:

- Microcontroller Applications and Advanced Microprocessors.

Course Objectives:

Microprocessors and microcontrollers play a very crucial role in all electronic systems

- To explain the need and application of ARM Microprocessors in embedded systems.
- To explore architecture and features of typical ARM7& ARM Cortex Processors
- To introduce of basics of the architecture of ARM series microprocessor, STM32F4xx
- To explore real world interfacing with STM32F4xx

Course Outcomes:

After successful completion of the course, the learner will be able to:

CO1: Apply knowledge about the basic functions of embedded systems.

CO2: Understand evolution of ARM from ARM7 to ARM11.

CO3: Understand basic architecture of ARM cortex STM32F4xx.

CO4: Interface advanced peripherals and design real time applications using ARM Cortex M4.

CO5: Evaluate case studies to explore design parameters and its selection in embedded applications.

Course Content:

UNIT-I: Introduction to Embedded Systems **08 Hours**

Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, design Metrics, General Purpose Processor.

Embedded system design and development: Embedded system design, Life-Cycle Models, Development tools.

Classifications: RISC, CISC, Flynn's Classification, Big and little endian CPI.

Computer Architecture: Pipelining stages, Superscalar processing, Throughput and latency.

UNIT-II: ARM architecture and Cortex – M series **09 Hours**

Introduction to ARM processors and its versions, ARM7, ARM9 & ARM11 features, advantages

& suitability in embedded application, registers, Firmware development using CMSIS Standard. Introduction to ARM CORTEX M4 microprocessor core, programmer model, Processor Modes, Memory Map, Introduction Arm Cortex-M cores.

UNIT-III: Architecture of STM32F4xx 08 Hours

STM32F4xx Architecture, ARM STM Bus Architecture, STM32F4xx Clock and SYSCLK, Peripheral Clock, PLL clock, Interrupts and Exceptions in STM32F4xx. GPIO Programming, STM32F4xx: Counters and Timers: Timer and Delay Generation.

UNIT-IV: Real world interfacing with STM32F4xx 08 Hours

Interfacing seven segment display , LCD with STM32F4xx, UART Programming, on chip ADC and On-chip DAC for waveform generation. PWM: Controlling speed and direction of DC Motor, Interfacing LDR, MPU 6050, and Ultrasonic Sensor HC-SR04 and MQ3 sensor with STM32F4xx.

UNIT-V: Embedded System Design Case Studies 08 Hours

Design Case Studies like Automated Meter Reading Systems (AMR), Digital Camera, Multimedia System, Electronic Control Unit (ECU) of Car and Medical Instrumentation.

Learning Resources:

1. David E. Simon, ―An Embedded Software Primer‖, Perason Education,2003.
2. Frank Vahid and Tony Givargis, ―Embedded System Design: A Unified Hardware/Software Introduction‖, Wiley Publication, 2006.
3. Microelectronic circuits: theory and applications" by A.S. Sedra and K.C. Smith, Adapted by A.N. Chandorkar, 6th Edition, Oxford, 2013.

Text Books:

1. Construction Planning & management By P S Gahlot & B M Dhir , New Age International Limited Publishers.
2. Construction Management – Roy, Pilcher.

Reference Books:

1. Noergaard Tammy, "Embedded Systems Architecture", Elsevier Publication.
2. Hallinan Christopher, "Embedded Linux Primer: A Practical Real-World Approach", Second Edition, Pearson Education.
3. Shibu,"Introduction to Embedded Systems", TMH.
4. Comer D E, " Network System Design using Network Process", PHI.
5. Croeley Patrick, Franklin M. A , Hadimioglu H &Onufryk P Z, "Network Processor Design, Issues and Practices", vol-1-2, Elsevier.

6. Uyless Black," Computer Networks-Protocols,Standards Interfaces",Second Edition ,PHI.
7. www.nxp.com/documents/user_manual/UM10360.pdf.
8. http://www.npforum.org/; http://www.intel.com/design/network/products/npfamily.

Web link for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/117101105

List of Experiments:

1. Interfacing of input devices with STM32F4xx
2. Interfacing of output devices with STM3232F4xx
3. Interfacing of different sensors with STM32F4xx
4. Serial communication for STM32F4xx
5. Programming with HAL and driver function of STM32F4xx

Course Code: 201104	Course Name: Research Methodology and IPR	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE : 50 Marks** **ESE : 50 Marks**

Prerequisite Courses:

- Students should complete undergraduate courses in engineering/technology.

Course Objectives:

- To provide an overview of the research problem and describe the functions of literature survey in research.
- To explain the statistical and probability analysis.
- To explain the art of writing research reports and papers.
- To understand the patenting process and its commercial aspects.
- To explain patent rights and new developments in IPR.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand research problem formulation, approaches of investigation of solutions for research problems and literature survey.

CO2: Apply the principles of statistics and probability analysis in research.

CO3: Acquire skills in research proposal/paper writing.

CO4: Discover the importance of IPR.

CO5: Understand patent rights and new developments in IPR.

Course Content:

UNIT-I: Research Problem and Literature Survey 11 Hours

Research Problem: Meaning of research problem, sources of research problem, characteristics of a good research problem, and errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problems, data collection, benchmarking, analysis, interpretation

Literature survey: Effective literature studies approaches, analysis, Plagiarism, its importance and software's, research ethics, research gap, writing objectives of research studies.

UNIT-II: Statistics and Probability Analysis 10 Hours

Statistical Analysis: Introduction, Sources of error and uncertainty, One-Dimensional Statistics:

combining errors and uncertainties, t-test, ANOVA statistics.

Probability Analysis: Classical and empirical probability, axioms of probability, conditional probability, Bayes' rule, law of total probability and law of total expectation.

UNIT-III: Technical Writing **11 Hours**

Characteristics of effective technical writing, developing a Research proposal, format of the research proposal, financial heads of the research project, research paper writing, abstracting and indexing of journals, impact factor, h index, research paper submission and review process, writing responses to reviewer's comments, Publications.

UNIT-IV: Intellectual Property **10 Hours**

Patents, designs, trade and copyright, the process of filing patents, designs, trade and copyright, examination, examination report, writing responses to the examination report, patent grant, commercialization, patenting under PCT and its advantages, case studies.

UNIT-V: Patent Rights and New Developments in IPR **10 Hours**

Scope of patent rights, Licensing and transfer of technology, patent information and databases, geographical Indications. Administration of patent system, new developments in IPR, IPR of biological systems, computer software etc.

Learning Resources:

1. Research Methodology: Methods and Trends, by Dr. C. R. Kothari.
2. Research Methodology: An Introduction by Wayne Goddard and Stuart Melville.
3. Research Methodology: A Step by Step Guide for Beginners, by Ranjit Kumar, 2nd Edition.
4. Halbert, Resisting Intellectual Property, Taylor & Francis Ltd.
5. Mayall, Industrial Design, McGraw Hill.
6. Niebel, Product Design, McGraw Hill.
7. T. Ramappa, Intellectual Property Rights under WTO, S. Chand.
8. Paul L. Meyer, Introductory probability and statistical applications, Addison-Wesley Publishing Company, 1970.

Web link for MOOC / NPTEL Links:

1. www.ipindia.gov.in
2. www.nptel.ac.in/courses/121106007

Course Code: 204105A	Course Name: Micro & Nano Electro-Mechanical Systems (MEMS & NEMS)	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Engineering Physics.

Course Objectives:

- Fundamental basis of MEMS/NEMS.
- Overview of basic micro-fabrication processes.
- MEMS-based sensors and actuators.
- Learn some typical or potentially applicable micro- and nano-systems at the frontier of the development of the field.

Course Outcomes:

On completion of the course, learner will be able to:

CO1: Describe the fundamentals of Micro Electro Mechanical Systems.

CO2: Able to design the micro devices, micro systems using the MEMS fabrication process.

CO3: Acquire an understanding of the fundamental methods for the design of a variety of sensors.

CO4: Acquire an understanding of fundamental methods for designing different actuators.

CO5: Summarize the applications of MEMS in real-world systems.

Course Contents:

UNIT-I: Introduction to MEMS & NEMS 11 Hours

Definition of MEMS and NEMS, their historical context, and key characteristics. Advantages and limitations of miniaturization. Overview of various MEMS and NEMS devices and applications.

UNIT-II: Micro-System Fabrication Processes 11 Hours

Micro-system fabrication photolithography, ion implantation, diffusion, oxidation, thin film depositions: LPCVD, sputtering, evaporation, electroplating; etching techniques: dry and wet etching, electrochemical etching; micromachining: bulk micromachining, surface micromachining, high aspect-ratio (LIGA and LIGA-like) technology; packaging: microsystems packaging, essential packaging technologies, selection of packaging materials.

UNIT-III: Micro Sensors 10 Hours

Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo-resistive Pressure sensors engineering mechanics behind these Micro-sensors.

Case Study: Piezo-resistive pressure sensor.

UNIT-IV: Micro Actuators 10 Hours

Design of actuators: actuation using thermal forces, actuation using shape memory alloys, actuation using piezoelectric crystals, actuation using electrostatic forces (parallel plate, torsion bar, comb drive actuators), micromechanical motors and pumps.

Case Study: Comb drive actuators.

UNIT-V: Applications of MEMS & NEMS 10 Hours

Case studies of MEMS and NEMS devices in various applications, including:

Automotive: Airbag deployment, navigation systems, and sensors for vehicle control.

Biomedical: Biosensors, drug delivery systems, and micro-fluidic devices.

Communication: Radio-frequency MEMS switches and antennas.

Consumer Electronics: Inkjet printers and digital micro-mirror devices.

Learning Resources:

Text Books:

1. Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997.
2. Stephen D. Senturia, Micro system Design, Kluwer Academic Publishers,2001.

Reference Books:

1. Tai Ran Hsu ,MEMS and Microsystems Design and Manufacture, Tata McGraw Hill, 2002.
2. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006
3. https://www.tutorialspoint.com/ngn/ngn_micro_electro_mechanical_systems.htm.

Weblink for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/117105082

Course Code: 204105B	Course Name: ASIC Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- VLSI fundamentals, Basic Analog & Digital Electronics.

Course Objectives:

- To understand different ASIC types, design methodologies, and tools.
- To gain knowledge of the physical design process and EDA tools.
- To explore various design constraints and optimization techniques.
- To apply Verilog/VHDL in the design and simulation of ASIC components.
- To examine fault tolerance and testing techniques for ASICs.

Course Outcomes:

On completion of the course, learner will be able to:

CO1: Understand the architecture, types, and applications of ASICs.

CO2: Apply design methodologies and tools for the development of ASICs.

CO3: Analyze and implement physical design steps including floor planning, placement, and routing.

CO4: Perform static timing analysis, delay estimation and synchronization.

CO5: Evaluate testing and verification strategies for robust ASIC development.

Course Contents:

UNIT-I: Introduction to ASICs **10 Hours**

Types of ASICs: Full-custom, semi-custom and programmable ASICs, ASIC design flow, comparison between ASICs and FPGAs, Overview of standard-cell based, gate-array based and structured ASICs, technology trends and applications.

UNIT-II: Design Methodologies for ASIC **10 Hours**

Design Entry: Schematic, HDL, simulation, synthesis, and floor-planning, partitioning and placement, clock tree synthesis, routing and layout, Design Rule Checking (DRC) and layout versus schematic (LVS).

UNIT-III: Physical Design **11 Hours**

System specifications, architecture design, logic and circuit design, physical design, CAD tools, system partitioning, estimating ASIC size, power dissipation, partitioning strategies, floor planning, placement, routing, design reuse.

UNIT-IV: Timing Analysis **10 Hours**

Static timing analysis, timing constraints, false path detection, timing optimization, ASIC library design, delay estimation, mixed mode design and simulation, SI issues.

UNIT-V: Verification and Testing for ASIC **11 Hours**

Different chip test methods, fault models, scan test, partial test, digital scan standards BIST architecture, memory testing, BILBO, boundary scan, self-test, JTAG, ATPG. Mixed signal ASIC design: mixed signal ASIC design, practical aspects of mix analog digital design, gate level mixed mode simulation. A brief introduction to signal integrity effects in ASIC design, synthesis and testing.

Learning Resources:

Text Books:

1. Michael John Sebastian Smith, “Application - Specific Integrated Circuits” Addison-Wesley Professional; 2005.
2. Singh Raminderpal, “Signal Integrity Effects in Custom IC and ASIC Designs”, Wiley Publications.

Reference Books:

1. Soin R S, Maloberti F, Franca J, “Analogue-digital ASICs: circuit techniques, design tools and applications”, IEE Publications.
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd edition, Addison Wesley/Pearson education, 2011
3. Vikram Arkalgud Chandra setty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations”, Springer, 2011, ISBN:978-1-4614-1119-2.
4. Rakesh Chadha, Bhasker J., “An ASIC Low Power Primer”, Springer, ISBN: 978-1-4614-4270-7.

Weblink for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/108106191
2. https://www.mooc-course.com/course-tag/asic-design/

Course Code: 204105C	Course Name: Embedded Automotive System	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Automotive electronics, Embedded systems, Control systems, Communication engineering.

Course Objectives:

- To introduce the potential of automotive systems in industries
- To understand Automotive Sensory Systems
- To explain the importance of Automotive control in system design
- To make student aware of different Automotive protocols for internal communication.

Course Outcomes:

On completion of the course, learner will be able to:

CO1: Analyze various embedded products used in the automotive industry.

CO2: Understand, design and model various automotive control systems using Model based development technique.

CO3: Understand networking of various modules in automotive systems and communication protocols of interfacing different electronics components, systems and functional counterparts.

CO4: Interface devices and build a complete automotive control system.

CO5: Use AUTOSAR software and functional safety norms for automotive design.

Course Contents:

UNIT-I: Automotive Systems Overview **11 Hours**

Automotive vehicle technology, overview of vehicle categories, various vehicle sub-systems like chassis, body, driveline, engine technology, fueling technology, vehicle emission, brakes, suspension, emission, doors, dashboard instruments, wiring harness, safety and security , comfort and infotainment, communication and lighting, future trends in automotive embedded systems: hybrid vehicles, electric vehicles.

UNIT-II: Automotive Sensory System **10 Hours**

Basics of advanced driver assistance systems, Radar technology and systems, ultrasonic sonar systems, Lidar sensor technology and systems, camera technology, night vision technology.

Proximity distance sensors, engine speed sensor, throttle position sensor, pressure sensors, knock sensor and mass flow sensor. Typical sensors specifications and microcontroller interface considerations, sensor calibration, curve fitting.

UNIT-III: Automotive Standards and Protocols 10 Hours

The need for protocol, LIN, CAN, KWP2000 & J1939, FlexRay, test calibration and diagnostics tools for networking of electronic systems like ECU, software and testing tools, ECU calibration tools, vehicle network simulation.

UNIT-IV: Automotive Control System Design 10 Hours

Digital engine control, features, control modes for fuel control, discrete time idle speed control, EGR control, variable valve timing control, electronic ignition control, integrated engine control system, summary of control modes, cruise control system, cruise control electronics, anti-locking braking system, electronic suspension system, electronic steering control, four-wheel steering.

UNIT-V: AUTOSAR and Functional Safety 11 Hours

Constituent elements of AUTOSAR, AUTOSAR methodology, system-level architectures & examples, functional safety, sw architectural descriptions for functional safety, hazard & risk analysis and determination of ASILs, futuristic trends in automotive electronics. Case study of modelling, simulation and implementation of automotive systems (Cruise control of car, Artificial Intelligence based ADAS system and engine management system).

Learning Resources:

Text Books:

1. William B. Ribbens, ―Understanding Automotive Electronics- An Engineering Perspective‖, Seventh edition, Butterworth-Heinemann Publications.
2. Tao Zhang, Luca Delgrossi—Vehicle Safety Communications: Protocols, Security and Privacy‖, Wiley Publication.
3. Nicolas Navet ―Automotive Embedded Systems Handbook‖, by, CRC press.

Reference Books:

1. Ronald K. Jurgen, "Automotive Electronics Handbook", Mc-Graw Hill.
2. Kiencke, Uwe, Nielsen & Lars, "Automotive Control Systems for Engine, Driveline and Vehicle", Second edition, Springer Publication.
3. Robert Bosch," Automotive Hand Book", Fifth edition, SAE Publications.

Weblink for MOOC / NPTEL Links:

1. https://www.coursera.org/learn/introduction-to-automotive-embedded-systems

Course Code: 204105D	Course Name: Electromagnetic Interference and Compatibility in ESD	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Basic understanding of electronics, circuit theory, embedded systems, and electromagnetic Field.

Course Objectives:

- Understand the fundamental principles & identify common sources.
- Practical design techniques for minimizing EMI and ensuring EMC.
- Interpret and apply global EMC standards.
- Test equipment and methods to detect, measure, and debug EMI/EMC issues.
- Design embedded systems that operate reliably in electromagnetically noisy environments.

Course Outcomes:

On completion of the course, learner will be able to:

CO1: Identify EMI sources and coupling mechanisms in embedded hardware and analyze their effects.

CO2: Apply EMI mitigation techniques.

CO3: Interpret and adhere to relevant EMC standards and regulations for embedded devices.

CO4: Use appropriate test instruments to evaluate and troubleshoot EMI/EMC issues.

CO5: Design and validate embedded systems that are EMC-compliant and function reliably.

Course Contents:

UNIT-I: EMI/EMC Concepts & Coupling Principles **10 Hours**

Sources of EMI: Classification, lightning, ESD, NEMP, conducted and radiated emission, conducted and radiated susceptibility, intra and inter system EMI, in band interference, spectrum conservation, radiation hazard, Specific Absorption Rate (SAR).

Conductive coupling: Common mode, differential mode, inductive coupling, capacitive coupling, radiative coupling.

UNIT-II: EMI Measurements **10 Hours**

Radiated Interference Measurements: Open area test site measurement, anechoic chamber, TEM cell, reverberating chamber.

Conducted Interference Measurements: Characterization of conduction currents voltages, conducted EM noise on power supply lines, conducted EMI from equipment, pulsed interference immunity: ESD/EFT, Electrical surge, time domain EMI measurement.

UNIT-III: EMI Control Methods and Fixes **11 Hours**

Grounding: Earthing principle, types of Grounding.

Shielding: Shielding theory and shielding effectiveness, shielding integrity at discontinuities, cable shielding.

Bonding: Shape and material for bond strap, general guidelines for good bonding. EMI Filters, Characteristics of filters, impedance mismatch effects, lumped element filters, common mode filter, differential mode filter, EMI suppression devices and components: EMI suppression cables, EMC connectors, EMC gaskets, isolation transformers, transient and surge suppression devices.

UNIT-IV: PCB Design for EMC Compliance **10 Hours**

PCB layout and stack up- multi layer PCB, return path discontinuities, mixed signal PCB layout. Board zoning, signal traces, cross talk, trace routing, cables and connectors. EMC pre-compliance measurement, conducted and radiated emission test-LISN.

UNIT-V: EMC Standards and Regulations **10 Hours**

National and Intentional standardizing organizations, FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and RE standards, CISPR, CE and RE Standards, IEC/EN, CS standards, frequency assignment, spectrum conversation.

Learning Resources:

Text Books:

1. Clayton R. Paul, Introduction to Electromagnetic Compatibility, WIS, 2022.
2. V. Prasad Kodali, “Engineering Electromagnetic Compatibility: Principles, Measurements, Technologies, and Computer Models”, Wiley-IEEE Press, 2001.

Reference Books:

1. H. W. Ott, Electromagnetic Compatibility Engineering, 2nd edition, John Wiley & Sons, 2011.
2. Christos Christopoulos, “Principles and Techniques of Electromagnetic Compatibility”, CRC Press, 2007.
3. Mark I. Montrose, “EMC Made Simple Printed Circuit Board and System Design”, Montrose Compliance Services, 2014.

Weblink for MOOC / NPTEL Links:

1. https://onlinecourses.nptel.ac.in/noc24_ee67/preview
2. https://www.mooc-list.com/course/electromagnetic-compatibility-essentials-edx

Course Code: 204106		Course Name: Skill Development Laboratory – I
Teaching Scheme	**Credit**	**Evaluation Scheme**
Practical : 2 Hours/Week	**1**	**TW : 25 Marks**

Prerequisite Courses:

- Basics of C, MATLAB, Python, VHDL.

Course Objectives:

- To strengthen the software programming skills of the students.
- To strengthen the hardware programming skills of the students.
- To develop knowledge of hardware and software co-design and to implement it on VLSI and Embedded platform.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand all the programming in the field of VLSI and Embedded Systems.

CO2: Design real time application using software and hardware tools.

CO3: Understand IC design and fabrication flow.

Course Contents:

Guidelines:

Total experiments to be conducted any three from Experiment 1 to 5 and any six from experiment 6 to 17.

List of Experiments:

1. Execute the Xilinx ISE tool design flow and verify for various modelling styles of VHDL with suitable examples on FPGA
2. Execute Vivado tool design flow and implement 4-bit counter using FPGA
3. Explore any two evaluation boards of FPGA / CPLD for interfacing with atleast two I/O modules such as Bluetooth, WAN, I2C, E2POM, ADC, DAC etc.
4. Execute Mentor graphics Tool HEP-I and HEP-II Design Flow with simple example.
5. Explore MATLAB Tool for adding new Toolbox and available libraries and execute HDL coder flow and System Generator flow of MATLAB for VHDL conversion.
6. **Serial Communication using UART**

Objective: Implement UART communication to send sensor data to a PC or another device.

Skills Developed: UART configuration, data framing, serial debugging.

Tools: UART + STM32

7. **Embedded System with Interrupts**

   Objective: Use external or internal interrupts to trigger events (e.g., button press, timer overflow).

   Skills Developed: ISR handling, edge triggering, low-latency response.

   Tools: STM32 with buttons or sensors

8. **Software Component (SWC) Design**

   Objective: Design a simple AUTOSAR SWC for a Headlamp Controller using provided port interfaces.

   Skills Developed: SWC development, interface definition, RTE interaction basics.

   Tools: AUTOSAR authoring tool (e.g., DaVinci Developer, EB Tresos Studio, or equivalent open-source tools)

9. **CAN Communication Stack Configuration**

   Objective: Configure the AUTOSAR CAN Stack (CanIf, CanDrv, CanSM, PduR) for a simple message exchange.

   Skills Developed: BSW module configuration, CAN transceiver integration, message routing.

   Tools: Vector DaVinci Configurator / EB Tresos / simulated CAN tools

10. **Electronic Throttle Control Simulation**

    Objective: Use PWM to simulate throttle control based on accelerator pedal position sensor.

    Skills Developed: PWM generation, ADC sensor reading, control logic.

    Tools: Potentiometer + Servo/DC motor + STM32

11. **Automotive Sensor Data Logging**

    Objective: Log and analyze data from automotive sensors (e.g., temperature, MAP, speed, Battery parameters) to SD card.

    Skills Developed: ADC, SD card interfacing, file system usage.

    Tools: STM32 + SD card module + sensors

12. **Anti-lock Braking System (ABS) Logic Simulation**

    Objective: Simulate ABS control logic using speed sensors (wheel encoder signals).

    Skills Developed: ISR for pulse counting, speed comparison, conditional control logic.

    Tools: Pulse generator or IR encoder + STM32

13. **LIN Bus Communication (Simulation)**

    Objective: Implement basic LIN communication between master and slave nodes.

    Skills Developed: Serial communication with LIN protocol rules, master-slave timing.

    Tools: UART + software-based LIN stack

14. **Engine Control Unit (ECU) Parameter Monitoring**

    Objective: Monitor and simulate ECU parameters such as air-fuel ratio, coolant temperature, etc.

    Skills Developed: Multi-sensor data handling, real-time display, decision making.

    Tools: STM32 + various sensors + display module

15. **AUTOSAR OS (OSEK/VDX) Task Scheduling**

    Objective: Create basic tasks (LED blinking, sensor reading) and schedule them using AUTOSAR OS configuration.

    Skills Developed: Task configuration in OIL file, OSEK concepts, real-time task handling.

    Tools: Trampoline RTOS (open-source AUTOSAR OS), FreeRTOS for concept comparison

16. **EMI Filter Design and Simulation**

    Objective: Design and simulate a filter to reduce switching noise and analyze attenuation.

    Skills Developed: Filter design for EMI, Impedance matching, Frequency response measurement

    Tool: Ansys HFSS / MATLAB Filter Design Toolbox

17. **Antenna Design and Placement:** Simulating the radiation patterns and performance of antennas, including minimizing unwanted emissions and ensuring proper placement to avoid interference with other components.

    Tool: Ansys HFSS

Learning Resources:

1. Xilinx ISE Simulation Guide https://www.xilinx.com/support/documentation/sw_manuals/xilinx14_7/sim.pdf
2. MATLAB user guide : https://in.mathworks.com/help/pdf_doc/matlab/index.html?s_tid=mwa_osa_a
3. Vivado User Guide: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug904-vivado-implementation.pdf

4. System Generator User Manual
https://www.xilinx.com/support/documentation/sw_manuals/xilinx11/sysgen_user.pdf
5. OMAP User Guide: https://www.ti.com/lit/ug/spruh77c/spruh77c.pdf
6. User Manual Code Composer Studio:
https://software-dl.ti.com/ccs/esd/documents/users_guide/index.html

Semester - II

Course Code:204201	Course Name: Analog CMOS Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 3 Hours/Week **Practical** : 2 Hours/Week	**3** **1**	**CCE** : 50 Marks **ESE** : 50 Marks **TW** : 25 Marks **OR** : 25 Marks

Prerequisite Courses:

- Analog Electronics.

Course Objectives:

- To understand the most important building blocks of all CMOS analog Ics.
- To study the basic principle of operation, the circuit choices and the tradeoffs involved in
- the MOS transistor level design common to all analog CMOS ICs.
- To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
- To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Design basic building blocks of CMOS analog ICs.

CO2: Carry out the design of single and two stage operational amplifiers and voltage references.

CO3: Determine the device dimensions of each MOSFETs involved.

CO4: Design various amplifiers like differential, current and operational amplifiers.

CO5: Design of BGR under low voltage conditions.

Course Content:

UNIT-I: MOS Devices and Modeling **08 Hours**

MOS transistor, passive components, capacitor & resistor, integrated circuit layout, CMOS device modeling, simple MOS large-signal model, other model parameters, small-signal model for the MOS transistor, computer simulation models, sub-threshold MOS model.

UNIT-II: Single Stage Amplifier **08 Hours**

CS stage with resistance load, divide connected load, Current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device

models.

Differential Amplifiers: Basic difference pair, Common mode response, differential pair with MOS loads, Gilbert cell.

UNIT-III: CMOS Operational Amplifiers **08 Hours**

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

UNIT-IV: Comparators **08 Hours**

Characterization of comparator, two-stage, open-loop comparators, other open-loop comparators, improving the performance of open-loop comparators, discrete-time comparators.

UNIT-V: Band Gap Reference **08 Hours**

General considerations, supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, band gap reference, PTAT generation, curvature correction, design of BGR under low voltage conditions.

Learning Resources:

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition.
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6th Edition.
3. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw Hill, 1994.
4. NeilH. Weste, David Money- CMOS VLSI Design: Acircuit&SystemPerspective",3 rd Edition Pearson Publication.
5. Tony Chan Carusone David A. Johns Kenneth W. Martin, Analog Integrated Circuit Design, Wiley, Second Edition (2011) CMOS Analog Circuit Design" by Phillip Allen and Douglas R. Holberg, OUP USA; Third Edition edition (1 September 2011)
6. Operation and Modeling of the MOS Transistor" by Yannis Tsividis, Oxford University, Press; 2 edition, June 26, 2003
7. "Microelectronic Circuits-Theory & Applications" by A.S. Sedra and K.C. Smith, Adapted by A.N. Chandorkar, 6th Edition, Oxford, 2013.

Reference Books:

1. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.
3. Paul G. A. Jespers and Boris Murmann, Systematic Design of Analog CMOS Circuits, Cambridge University Press, 2017.

Web link for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/117101105

List of Experiments:

At the end of the laboratory work, students will be able to design analog Circuit using CMOS and use EDA tools like Cadence, Mentor Graphics and other open-source software tools like Ngspice

1. Use VDD = 1.8V for 0.18 um CMOS process, VDD = 1.3V for 0.13 um CMOS Process and VDD = 1V for 0.09 um CMOS Process.
   a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
2. Tabulate your result according to technologies and comment on it.
3. Use VDD = 1.8V for 0.18 um CMOS process, VDD =1.2V for 0.13 um CMOS Process and VDD = 1V for 0.09 um CMOS Process.
   a. Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
4. Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18 um and 0.13 um technology and compare its frequencies and time period.
5. Built Three OP-AMP INA. Vdd = 1.8V Vss = 0V, CAD tool: Mentor Graphics DA.

   Note: Adjust accuracy options of the simulator (setup->options in GUI).

Course Code: 204202	Course Name: Device Modelling for VLSI	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Fundamentals of Analog and Digital circuits.

Course Objectives:

Explicate the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modelling and physics of various carrier current transport mechanisms

- Familiarize detailed physics and modelling of PN Junction, MOS capacitors, and MOSFETs
- To study the impact of scaling on device performance and reliability ·
- To understand the characteristics of the Fin-FETs and its applications
- To model and implement the devices from basic characteristics to performance evaluation.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Analyze the principles of semiconductor physics, including carrier concentrations and current flow mechanisms.

CO2: Develop an understanding of MOS capacitors and MOSFET characteristics, implementing compact models in SPICE for circuit simulation, and solving practical design challenges.

CO3: Analyze the effects of scaling and short-channel effects on MOSFET performance in modern semiconductor devices, investigating their implications on real-world designs.

CO4: Use the Fin-FET for various applications.

CO5: Understand performance analysis of fabricated chips.

Course Contents:

UNIT-I: Semiconductor Physics and Carrier Transportation 11 Hours

Energy bands in intrinsic and extrinsic semiconductors, direct and indirect semiconductors, carrier concentrations, density of states, Fermi-Dirac distribution, temperature dependence of carrier concentrations, compensation and space charge neutrality.

Current Flow Mechanisms: Mobility, drift current, diffusion current, current density equations, continuity equation.

UNIT-II: MOS Capacitor, MOSFETs and Compact Models 11 Hours

MOS Capacitor: accumulation, depletion, week inversion, strong inversion, channel length modulation, gate work function, oxide and interface charges, threshold voltage, current-voltage **Characteristics of MOS MOSFETs:** Drain current, saturation voltage, sub-threshold conduction, effect of gate and drain voltage on carrier mobility, compact models for MOSFET and their implementation in SPICE.

UNIT-III: Scaling and Short Channel Effects 10 Hours

Short channel MOSFET, small dimension effects, channel length modulation, barrier lowing two-dimensional charge sharing and threshold voltage, punch through, carrier velocity saturation, hot carrier effects, scaling, effects due to thin oxides and high doping, mobility degradation.

UNIT-IV: Fin-FETs 10 Hours

I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using Fin-FETs and GAA devices.

UNIT-V: CMOS Fabrication Technology 10 Hours

An overview of wafer fabrication, oxidation, photo lithography, diffusion, ion implantation, metallization, packaging, n-MOS process, n well CMOS process, p well CMOS process, twin-tub process, silicon on insulator process, Bi-CMOS process.

Learning Resources:

Text Books:

1. YannisTsividis, “Operation and modeling of the MOS transistor”, Oxford University Press
2. Kang S. M , “CMOS Digital Integrated Circuits”, Tata Mc-Graw Hill.
3. Carlos Galup & Montoro, “MOSFET Modeling for Circuit Analysis and Design”, World Scientific.
4. Donald Neamen, “Semiconductors Physics and Devices”, Tata Mc-Graw Hill. 5. Sze S. M, “Physics of Semiconductor Devices, Second Edition, Wiley Publications.

Reference Books:

1. S. M. Sze, “Physics of Semiconductor Devices”, 2nd Ed., Wiley Eastern, 1981.
2. Y. P. Tsividis, “Operation and Modelling of the MOS Transistor”, McGraw-Hill, 1987.
3. E. Takeda, “Hot-carrier Effects in MOS Transistors”, Academic Press, 1995.
4. P. Colinge, “FinFETs and Other Multi-Gate Transistors”, Springer. 2009.

Web link for MOOC / NPTEL Links:

1. https://onlinecourses.nptel.ac.in/noc21_ee09/preview

Assignments:

1. Characterize n-MOSFET with the given model parameters, from the parameters students will reproduce I-V characteristics. Replace the model with any other SPICE model. Compare both the I-V characteristics.
2. Characterize p-MOSFET with the given model parameters, from the parameters students will reproduce I-V characteristics. Replace the model with any other SPICE model. Compare both the device I-V characteristics.
3. Characterize n-MOSFET and p-MOSFET to find out low frequency C-V characteristics behavior with the given model parameters.
4. Characterize n-MOSFET and p-MOSFET to find out high frequency C-V characteristics behavior with the given model parameters.
5. Demonstration of Implementation of Fin-FET in Micro wind
6. Implementation of Basic gate using QCAD
7. Case study on SET for Ultra- low power Design.

Course Code: 204203	Course Name: Real Time Operating System	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week **Practical** : 2 Hours/Week	**4** **1**	**CCE** : 50 Marks **ESE** : 50 Marks **TW** : 25 Marks

Prerequisite Courses:

- Embedded System.

Course Objectives:

- To provide a foundational understanding of operating system architecture, functions, and the system boot process.
- To introduce the principles of real-time systems and scheduling algorithms, with a focus on their applications in embedded and Linux-based environments.
- To develop the ability to implement inter-process communication, synchronization techniques, and explore Embedded Linux system components and RTOS case studies.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Explain the structure, functions, and kernel architectures of an operating system along with the booting process.

CO2: Classify real-time systems and apply appropriate scheduling algorithms for real-time task management.

CO3: Implement inter-process communication and synchronization techniques to avoid race conditions and ensure process coordination.

CO4: Analyze the components of Embedded Linux systems and outline the steps to develop or port Linux on embedded hardware platforms.

CO5: Configure and deploy Free RTOS on STM32 platforms using STM32CubeMX, and examine hardware-level task management.

Course Content:

UNIT-I: Introduction to OS **10 Hours**

Layers of operating system, operating system function, system boot up – BIOS & Boot Process.

Kernel Architectures: Monolithic, Microkernel, hybrid, RTOS basics.

UNIT-II: RTOS Concept & Scheduling 11 Hours

Real-Time System: Types, examples, process management and scheduling basics: Task states and life cycle. Clock-driven and event-driven scheduling.

Fixed-Priority Scheduling: RMS, deadline monotonic,

Dynamic Scheduling: EDF, Least Laxity First. Linux RT Scheduler, Issues in Real-Time Scheduling.

UNIT-III: IPC – Synchronization 11 Hours

IPC, Race Condition & Critical Condition, Signals, Atomic Operation, Semaphore, Mutex, Spinlock , Priority Inversion and Priority Ceiling. Shared Memory, FIFO, Message and Mailbox, Circular and Sliding Buffers, RPC.

Case Studies of MicroC/OS-II, VxWorks, Tiny OS and Basic Concept of Android OS.

UNIT-IV: Embedded Linux 10 Hours

Embedded Linux: Linux for embedded systems, embedded Linux development system, kernel architecture and configuration, file systems, porting Linux on ARM architecture, boot loaders, tool utilities such as Minicomp, Busybox, Redboot, Libc, Device drivers-concept, architecture, types, sample character device driver.

Case Studies of RT Linux, Embedded Linux.

UNIT-V: RTOS for STM32F4 10 Hours

Introduction to Free RTOS. Configure FreeRTOS Using STM32CubeMX, Thread Management, Free RTOS and the C stdlib, Synchronization Primitives, Debugging features of Free RTOS, debugging with STM32CubeIDE. Alternatives open source RTOS to Free RTOS: ChibiOS and Contiki OS. Create a Free RTOS project in STM32CubeIDE. Write C code for any task/event/thread with Free RTOS.

Learning Resources:

Text Books:

1. Rajkamal, Embedded Systems: Architecture, Programming and Design, Tata McGraw-Hill Education, 2008
2. Labrossy J. J, Lawrence, ―µC/OS-II, The real time Kernel‖, R & D Publication.
3. Hallinan Christopher, ―Embedded Linux Primer: A Practical Real-World Approach‖, Second Edition, Pearson Education, 2006.

Reference Books:

1. Frank Vahid and Tony Givargis, "Embedded system design: a unified hardware/software Introduction",Wiley , 2002.
2. Tanenbaum A S, ―Modern Operating Systems‖, 4e, Prentice Hall, 2015.
3. Real-Time Concepts for Embedded Systems – Qing Li
4. Chris Simmonds, "Master the techniques needed to build great, efficient embedded devices on Linux"
5. Carmine Noviello, "Mastering STM32", 2nd Edition, Lean Publisher.
6. RM0390 Reference manual, STM32F446xx advanced Arm®-based 32-bit MCUs.

Web link for MOOC / NPTEL Links:

1. IEEE Transactions on Computers, Embedded Systems Letters, RTSS Conference Proceedings.

List of Experiments:

1. Multitasking in µCOS II RTOS using minimum 3 tasks.
2. Semaphore as signaling & Synchronizing
3. Mailbox implementation for message passing
4. Queue implementation for message passing
5. Implementation of MUTEX using minimum 3 tasks
6. Porting of linux operating system.
7. Configure FreeRTOS Using CubeMX.
8. Interfacing of LoRaWAN with STM32F4.

Course Code: 204204A	Course Name: System on Chip Design	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Fundamentals of VLSI.

Course Objectives:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the design of embedded memories.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Able to understand about SoC Design methodology.

CO2: Ability to understand the design of different embedded memories.

CO3: Validation and testing concepts can be understood.

CO4: Validation and testing concepts can be understood.

CO5: Investigate new techniques for future systems.

Course Contents:

UNIT-I: Introduction **09 Hours**

System trade-offs and evolution of ASIC Technology, System on chip concepts and methodology – SoC design issues -SoC challenges and components.

UNIT-II: Design Methodological For Logic Cores **11 Hours**

SoC design flow, on-chip buses, design process for hard cores, soft and firm cores, core and SoC design examples.

UNIT-III: Design Methodology for Memory and Analog Cores **10 Hours**

Embedded memories, simulation modes, specification of analog circuits – A to D converter, phase locked loops, High I/O.

UNIT-IV: Design Validation 11 Hours

Core level validation, test benches, SoC design validation, co-simulation, hardware software co-verification. Case Study: Validation and test of systems on chip.

UNIT-V: SOC Testing 11 Hours

SoC Test Issues, cores with boundary scan – test methodology for design reuse, testing of microprocessor cores, built in self-method testing of embedded memories.

Learning Resources:

Text Books:

1. Rochit Rajsunah, System-on-a-chip: Design and Test, Artech House,2007.
2. Prakash Raslinkar, Peter Paterson &Leena Singh, System-on-a-chip verification: Methodology and Techniques, Kluwer Academic Publishers, 2000.

Reference Books:

1. M. Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on- Chip Design Series: Integrated Circuits and Systems, Springer,2007.
2. Balado, E. Lupon, Validation and test of systems on chip, IEEE conference on ASIC/SOC,1999.
3. A. Manzone, P. Bernardi, M. Grosso, M. Rebaudengo, E. Sanchez, M. S Reorda, Centro Ricerche Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing, 2000.

Web link for MOOC / NPTEL Links:

1. https://elearn.maven-silicon.com/course/vlsi-system-on-chip-design-8

Course Code: 204204B	Course Name: VLSI Testing and Testability	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Fundamentals of VLSI.

Course Objectives:

- To understand challenges in VLSI Testing at different abstraction levels.
- To understand the logical and fault simulation models
- To learn techniques for design of testability
- To study hardware and software verification issues for testing
- To study verification plan for testing.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand fault models for generation of test vectors.

CO2: Calculate observability and controllability parameters of circuit.

CO3: Enhance testability of a circuit.

CO4: Use simulation techniques for designing and testing of VLSI circuits.

CO5: Identify characteristics of verification methods.

Course Contents:

UNIT-I: Introduction to Testing 09 Hours

Testing philosophy, role of testing, digital and analog vlsi testing, vlsi technology trends affecting testing. Faults in digital circuits: failures and faults, modeling of faults, temporary faults. Test generation for combinational logic circuits: fault diagnosis of digital circuits, test generation techniques for combinational circuits, detection of multiple fauls in combinational logic circuits.

UNIT-II: Design for Testability 11 Hours

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Non scan Techniques, Cross

Check, Boundry Scan. Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures. Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

UNIT-III: Design Verification **11 Hours**

Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification. **Verification Tools:** Linting tools: Limitations of linting tools, linting Verilog source code, linting VHDL source code, linting Open Vera and e-source code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle-based simulation, Co-simulators, verification. **Intellectual Property:** Hardware modelers, waveform viewers.

UNIT-IV: Verification Plan **11 Hours**

Role of Verification Plan: specifying the verification plan, defining the first success. Levels of verification: Unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. **Physical Design Verification:** Layout rule checks and electrical rule checks. Parasitic extraction. **Antenna, Crosstalk and Noise:** Cross talk glitch analysis, crosstalk delay analysis, timing verification.

UNIT-V: Static Timing Verification **08 Hours**

Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs, Min and Max timing paths, clock domains, operating conditions, critical path analysis, false paths, Timing models.

Learning Resources:

Text Books:

1. Bushnell M L, Agrawal V D, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
2. Abramovici M, Breuer M A and Friedman A D, “Digital systems and Testable Design”, Jaico Publications, 2002.
3. P. K. Lala, ―Digital Circuit Testing and Testability‖, Academic Press, 1997.

Reference Books:

1. Crouch A L, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall
2. Kropf T, “Introduction to Formal Hardware Verification”, Springer Publications
3. Jayaram Bhasker and Rakesh Chadha, ―Static Timing Analysis for Nanometer Designs‖ A practical approach, 1st Edition, Springer publications, 2009.

Web link for MOOC / NPTEL Links:

1. https://onlinecourses.nptel.ac.in/noc25_ee25/preview
2. https://nptel.ac.in/courses/106103016

Course Code: 204204C	Course Name: Embedded System for Biomedical	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- Microcontroller, Embedded C, MATLAB.

Course Objectives:

- To provide the knowledge of basic concepts such as measuring instruments and generalized instrumentation system, general properties of input transducers, static and dynamic characteristics of transducers and sensors.
- To deliver knowledge of Signal Processing and Time-frequency transforms required for biomedical processing and data mining.
- To give the students an understanding of Bioelectric signals, electrodes and its dynamics.
- To introduce biomedical pre-processing methodologies, instrumentation and its applications.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand sensors and electrodes for biomedical signal recording.

CO2: Understand concept of bio-electric signals such as EEG, ECG and EMG and its relevance for normal and abnormal state.

CO3: Design real time pre-processing system required for medical signal processing and medical imaging.

CO4: Understand medical imaging concepts for disease analysis.

CO5: Design automated, handheld embedded systems used in society for addressing health and hygiene challenges.

Course Contents:

UNIT-I: Introduction to Biomedical Signals **10 Hours**

Origins of Bioelectric signals, Electrocardiogram (ECG), Electromyogram (EMG); Recording Electrodes- Silver-silver Electrodes, Electrodes for ECG, EEG and EMG; electrodes types and selection of Sensors.

Recording Electrodes: Electrode-tissue interface, polarization, skin contact impedance, effects of artifacts, Silver-Silver Chloride electrodes, Electrodes for ECG, Electrodes for EEG, single

channel and multi-channel EEG, Electrodes of EMG. Electrical Conductivity of Jellies and Creams, Microelectrodes.

UNIT-II: Signal Processing for ECG 11 Hours

ECG signal origin, ECG parameters-QRS detection different techniques, ST segment analysis. Signal averaging: Basics of signal averaging, Signal averaging as a digital filter, A typical averager, Software and limitations of signal averaging. Adaptive Filtering: Introduction, General structure of adaptive filters, LMS adaptive filter, adaptive noise cancellation, Cancellation of 60Hz interference in ECG, Cancellation of maternal ECG in fetal ECG.

UNIT-III: Frequency Domain Analysis 11 Hours

Introduction, Spectral analysis, linear filtering, cepstral analysis and homomorphic filtering. Removal of high frequency noise (power line interference), motion artifacts (low frequency) and power line interference in ECG / EEG.

Time Series Analysis: Introduction, AR models, Estimation of AR parameters by method of least squares and Durbin‘s algorithm, ARMA models. Spectral modeling and analysis of PCG (Phonocardiogram) signals.

UNIT-IV: Medical Imaging 10 Hours

Magnetic Resonance Imaging: Introduction, principles of MRI and fMRI, MRI instrumentation, image acquisition and reconstruction techniques, Application of MRI.

UNIT-V: Data Acquisition and Case Studies 10 Hours

Introduction, Measurement and Automation Explorer, DAQ Assistants, Analysis Assistants. Biomedical toolkit- ECG signal acquisition & feature extraction, EEG simulation, EMG power analysis. Image acquisition and processing, Patient Monitoring Systems, Intelligent Health care system, Telemedicine.

Learning Resources:

Text Books:

1. J.C. Proakis & M.G. Manslakis Digital Signal Processing: Principles, Algorithms & Application, ,PHI
2. Arnon Cohen, Biomedical Signal Processing Time and Frequency Domains Analysis (Volume I), ,Edition, 1986, CRC press, ISBN:978-1-111-42737-5.
3. D.C.Reddy , Biomedical Signal Processing Principles and Techniques, Tata McGraw-Hill, ISBN: 978-1- 111-42737-5,2012.

Reference Books:

1. MR. S. Khandpur , Handbook of Biomedical Instrumentation, 3 rd Edition, 2011, Tata Mc Graw-Hill ,ISBN: 9780070473553.

2. Willis J. Tompkins, Biomedical Digital Signal Processing, , edition, 2000, PHI, ISBN: 978-1-111-42737-5
3. E.S. Gopi, Digital Signal Processing for Medical Imaging Using Matlab, Springer, 2013.

Web link for MOOC / NPTEL Links:

1. https://nptel.ac.in/courses/108102045
2. https://onlinecourses.nptel.ac.in/noc22_cs93/preview

Course Code: 204204D	Course Name: Security in Embedded System	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Theory : 4 Hours/Week	**4**	**CCE :** 50 Marks **ESE :** 50 Marks

Prerequisite Courses:

- VLSI Design Flow, Basics of FPGA.

Course Objectives:

- To explore software and hardware-based security techniques
- To study secure boot, trusted execution environments (TEEs), and hardware security modules
- To apply cryptographic techniques in constrained environments.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Identify security threats in embedded and IoT systems.

CO2: Analyze cryptographic techniques suitable for constrained environments.

CO3: Explore secure hardware and software design methodologies.

CO4: Implement secure communication protocols and update mechanisms.

CO5: Analyze real-world case studies and current research trends.

Course Contents:

UNIT-I: Introduction to Embedded Security 10 Hours

Overview of embedded systems and their security needs, Importance of security in IoT, automotive, medical devices. **Threat models:** physical attacks, side-channel attacks, reverse engineering, Security lifecycle in embedded systems, Real-world examples of security breaches in embedded systems. **Case studies:** Automotive, IoT, and medical devices.

UNIT-II: Cryptography for Embedded Systems 11 Hours

Symmetric and asymmetric cryptography basics, Symmetric key cryptography: AES (Advanced Encryption Standard), Asymmetric key cryptography: RSA and ECC (Elliptic Curve Cryptography), Hash functions (SHA-256) and digital signatures, Lightweight cryptography (e.g., PRESENT, HIGHT, SPECK), Key generation, storage, and management in embedded devices, Public Key Infrastructure (PKI) in constrained environments, Secure random number generation

and TRNGs.

UNIT-III: Secure Hardware and Software Design 11 Hours

Importance of firmware security, Trusted Platform Modules (TPM), Hardware Security Modules (HSM), Secure boot, secure update mechanisms, Memory protection and access control techniques, Firmware and OS security (e.g., Secure RTOS), Secure key storage: eFuses, TPM (Trusted Platform Module), Physically Unclonable Functions (PUFs): concept and use, Anti-tamper techniques in embedded design, Trust models in SoC design.

UNIT-IV: Communication Security 11 Hours

Basic principles of secure communication, Secure communication protocols: TLS/DTLS, MQTT with TLS, CoAP, ZigBee, LoRaWAN, Authentication and authorization in networked embedded systems, Key exchange and authentication, Wireless network vulnerabilities and countermeasure.

UNIT-V: Attacks, Countermeasures, and Testing 09 Hours

Hardware Attacks: fault injection, power analysis, EM analysis, Software attacks: buffer overflow, code injection, malware in firmware. **Basic Protection Methods:** masking, random delays, Secure coding standards for embedded systems, Penetration testing and vulnerability assessment tools.

Learning Resources:

Text Books:

1. "Security in Embedded Systems" by D. Mukhopadhyay and R. S. Chakraborty.
2. "Embedded Systems Security: Practical Methods for Safe and Secure Software and Systems Development" by D. Kleidermacher
3. "Introduction to Hardware Security and Trust" by Mohammad Tehranipoor
4. "Cryptography and Network Security" by Atul Kahate Tata McGraw-Hill.

Reference Books:

1. Security in Embedded Devices" – Dr. C. Y. Hung
2. "Cryptography and Network Security" by William Stallings Pearson Education India
3. Hardware Security: Design, Threats, and Safeguards" by Debdeep Mukhopadhyay, Rajat Subhra Chakraborty Indian Reprint available
4. Embedded Systems Security, David Kleidermacher & Mike Kleidermache.

Web link for MOOC / NPTEL Links:

1. https://www.edx.org/learn/embedded-systems
2. https://www.coursera.org/learn/iot-connectivity-security

Course Code: 204205		Course Name: Skill Development Laboratory – II
Teaching Scheme	**Credit**	**Evaluation Scheme**
Practical : 2 Hours/Week	**1**	**TW : 25 Marks**

Prerequisite Courses:

- Basics of C, MATLAB, Python, VHDL.

Course Objectives:

- To strengthen the software programming skills of the students.
- To strengthen the hardware programming skills of the students.
- To develop knowledge of hardware and software co-design and to implement it on VLSI and Embedded platform.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Understand all the programming in the field of VLSI and Embedded Systems.

CO2: Design real time application using software and hardware tools.

CO3: Understand IC design and fabrication flow.

Guidelines:

1. Total activities to be conducted are four out of five.
2. Total: five activities in 15-20 hours.

List of Practicals:

Total eight experiments from Experiment 1 – 11.

1. **Study of Sensor Data Sharing using Queues**

   Objective: Task 1 reads data from a sensor (e.g., LM35), and Task 2 logs it to serial using Free RTOS queues.

   Skills Developed: Inter-task communication, xQueueSend(), xQueueReceive().

   Tools: Free RTOS.

2. **Semaphore-Controlled Resource Access**

   Objective: Use binary semaphore to control access to a shared UART or SPI peripheral.

   Skills Developed: Binary semaphores, mutual exclusion, race condition prevention.

   Tools: Free RTOS.

3. **Assignment 3: Priority Inversion Simulation and Solution**

Objective: Create a scenario with priority inversion and resolve it using priority inheritance with mutexes.

Skills Developed: Mutex usage, task starvation prevention, debugging priority issues.

Tools: Free RTOS.

4. **Assignment 4: Producer-Consumer using RTOS Queues**

   Objective: Producer task generates data (e.g., ADC values), consumer task processes it.

   Skills Developed: Queue buffer management, blocking queues

   RTOS Concept: Synchronization, resource sharing

   Tools: Free RTOS + Sensor + Display/Log

5. **Assignment 5: Interrupt Handling with Task Notification**

   Objective: Trigger a task from an external interrupt (e.g., button press) using task notification.

   Skills Developed: xTask Notify From ISR, ISR-to-task signaling

   RTOS Concept: Task notification, ISR integration ,Tools: STM32 + Push button

6. **Assignment 6: Patient Health Monitoring System**

   Objective: Measure and display real-time heart rate, temperature and SpO2.

   Skills Developed: ADC interfacing, analog signal processing, real-time display.

   Tools: Pulse Sensor + temperature sensor + SpO2 sensor + STM32 + OLED/LCD

7. **Assignment 7: Biomedical Data Logger**

   Objective: Design a wearable device prototype to monitor vitals and transmit via Bluetooth.

   Skills Developed: Embedded IoT, BLE communication, low-power design.

   Tools: ESP32 + STM32 +BLE + Sensors + Mobile App

8. **Assignment 8: ECG Signal Acquisition and Display**

   Objective: Acquire ECG signal using analog front-end and display waveform on serial plotter or display.

   Skills Developed: Analog signal acquisition, filtering, noise handling.

   Tools: AD8232 ECG Module + STM32/Arduino + Serial Monitor

9. **Assignment 9: Embedded Intrusion Detection System (IDS) Prototype**

   Objective: Simulate a basic IDS by monitoring unauthorized data patterns or behavior and triggering alerts.

   Skills Developed: Real-time monitoring, Rule-based detection, Alert generation

   Tools: STM32 / ESP32 + motion sensor / UART + buzzer or GSM module

10. **Assignment 10: Embedded Firewall Rule Simulation**

    Objective: Simulate a basic firewall inside a microcontroller that filters or blocks unwanted UART/CAN messages based on ID or content.

    Skills Developed: Packet inspection, Rule-based filtering logic, CAN/UART bus monitoring.

    Tools: STM32 + Python + pySerial (for UART traffic simulation)

11. **Assignment 11: Firmware Update Verification via Digital Signature**

    Objective: Create a method to verify firmware updates using digital signature verification before allowing updates.

    Skills Developed: Public key cryptography concepts, Embedded signature check (RSA, ECC simulated), Firmware version control and validation

    Tools: STM32 + QEMU (for simulating embedded processors).

Learning Resources:

Text Books:

1. Mastering STM32 - Second Edition , A step-by-step guide to the most complete ARM Cortex-M platform, using the official STM32Cube development environment. Carmine Noviello.
2. ESP32 Programming for the Internet of Things - Second Edition: HTML, JavaScript, MQTT and WebSockets Solution by Sever Spanulescu.

Reference Books:

1. Hands-On RTOS with Microcontrollers: Building real-time embedded systems using Free RTOS, STM32 MCUs, and SEGGER debug tools Paperback – 15 May 2020 by Brian Amos.

Web Link for MOOC / NPTEL / YouTube Links:

1. https://onlinecourses.nptel.ac.in/noc25_ee31/preview

Course Code: 204206	Course Name: Seminar	
Teaching Scheme	**Credit**	**Evaluation Scheme**
Practical : 4 Hours/Week	**2**	**TW : 50 Marks** **OR : 50 Marks**

Course Objectives:

- To identify the latest topic in the field of design engineering
- To carry out literature surveys and problem identification
- Enhance presentation and report writing skills.

Course Outcomes:

After successful completion of the course, learner will be able to:

CO1: Identify the seminar topic in the field of design engineering by literature survey.

CO2: Understand how research papers are written and understand modeling, theory, concept, and simulation related to the topic of interest.

CO3: Effectively communicate the seminar topic through oral presentation.

CO4: Prepare a detailed seminar report.

Course Contents:

Seminar-I topic will be based on current research in the field of Electronic and Telecommunication Engineering case study approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work by the concerned Guide and head of the department.

Guidelines:

Seminar shall be on any related topic of specialization approved by a guide/authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work by the concerned guide and head of the department/institute.

1. Individual student needs to study recent topics in the field of electronics and telecommunication engineering under the guidance of allocated guide.
2. Students can choose topic related to electronics and telecommunication engineering, considering recent trends and its societal importance.
3. The extensive literature survey, mathematical modeling of particular method, experimentation and valuable conclusion is expected from seminar study.
4. Seminar report should be submitted as a compliance of term work.

5. Technical paper publication is expected as outcome of seminar.
6. Total duration: 24 contact hours and additional 24 hours should be spend by students on completion of related activities and requirements.

Course Contents

Week	Activities
1 and 2	Guide allotment and finalization of topic (Review 1)
2 and 3	Literature review, objectives and planning of the work.
4 and 5	Literature review, methodology finalization.
5 and 6	Detail topic data collection, mathematical model, case study analysis, experimentation methodology and findings. (Review 2)
6 to 8	Result and discussion, solutions to the identified problem or research gaps.
9 to 12	Seminar report writing, preparation of presentation and publication or copyright planning, final Review conduction.