



MARATHA VIDYA PRASARAK SAMAJ'S

**Karmaveer Adv. Baburao Ganpatrao Thakare  
College of Engineering, Nashik**

NBA



### Department of Information Technology

Academic Year :- 2022-23	Class:- Second Year
Semester :- II	Date :- 30-9-2022
CO :- CO3	PO :- PO1,PO2,PO3,PO5,PO9,PO10

**1. Name of Innovative Method: Build and simulate logic circuits with Easiest way**

**2. Name of Faculty: - Dr. Jaya R. Suryawanshi**

**3. Subject: LDCO**

**4. Objective of Method:**

This method can be used as an effective means for teaching or demonstrating concepts to students. Simulation dynamically shows the behavior and relationship of all the simulated system's components, thereby providing the students with a meaningful understanding of the system.

**5. Topic Covered through Activity:**

Scheduling Algorithms – Unit 1, Unit 2, Unit 3.

**6. Description of method with Benefits:**

In this method students select the any digital electronics circuit. They use the simulator to design and implement the circuit diagram. They present it in front of class. A simulator which permits the construction, interconnection and subsequent simulation of the higher level entities is in such an easiest way, so the students can build and connect simple logic gates for implementation of any digital circuit.

**Method:**

In this method, student will be design and implement digital electronics circuit using simulator and demonstrate it for other students.

**Roles and Responsibilities:**

**• Teacher:**

- Define rubrics for the assessment of the activity.
- Assign different digital circuit to students.
- Assess the reports.

**• Student:**

- o Go through the provided circuit and understand the basic need to design this circuit.
- o Student should be able to demonstrate their circuit in front of all students.

#### 7. Assessment Rubrics:

Sr. No	Name of Method	Evaluation Criteria	SC	Excellent	Satisfactory	Poor
01		Timely Submission	02	Within specific defined Time period (2M)	More time than specific (1 M)	Extra time than defined. (0M)
		Demonstration	4	All input output functions are completely (100%)working (4 M)	All input output functions are completely (80%)working (3 M)	All input output functions are completely (50%)working (0 - 2M)
		Question Answer	4	Appropriate Answers to Questions. (4 M)	Answers questions, but often with little insight. (3 M)	Inappropriate Answers (0 - 2M)

#### 8. Evaluation Sheet

Group No	Roll No	Name	Topic	Demonstration (4)	Question Answer (4)	Timely Submission (2)	Total (10)
1	01	HARSHALI SANJAY AHIRE	4 bit BCD to Excess 3 code conversion	4	3	2	9
	02	PRATIKSHA SANDIP AHIRE		4	3	2	9
	16	RASHIMI SHAM GHORPADE		4	3	2	9
2	23	VIDYA DATTU KEKAN	Full Adder	4	3	2	9
	31	MANASI RAHUL MAHAJAN		4	3	2	9
	33	DIVYA BHAGWAT MAHAJAN		4	3	1	8
	34	SANJANA MANGESH MAHALE		4	3	2	9
3	40	NIKHIL SAMADHAN NIKAM	Half Adder	3	3	2	8
	30	RUSHIKESH RAJENDRA KUSHARE		3	3	2	8
	12	YASH SHARAD DEORE		3	3	2	8
	45	YASH SACHIN PATIL		3	3	2	8
4	34	SAYALI ARVIND MARATHE	BCD adder	3	3	2	8
	41	PAYAL BHAGWAT PADMANE		3	3	3	9
5	57	DIVYA VISHWANATH SHEWALE	BCD adder	2	3	2	7
	43	SNEHA SHANKAR PARDESHI		3	3	2	8
	58	KUNAL POPATRAO SHEWALE		3	3	3	9

	21	OM VIJAY KAPADNIS		3	3	2	8
	03	DIHRAJ PANDHIRINATHI BAGUL		3	3	3	9
6	64	VARAD PANDURANG SURYAWANSHI	4 bit conversion	3	3	2	8
	65	AVISIKAR ARJUN TATHE		3	3	3	9
	66	AJIT POPAT THAKARE		3	3	3	9
7	9	SAMIKSHA DIPAK BRAMHANKAR	BCD adder	3	3	2	8
	11	TEJASVINI VIDAY DANDGE		3	3	2	8
	61	YASHASHRI SANJAY SHINDE		3	3	2	8
8	39	OM SATISHCHANDRA NIKAM	Half Adder	3	3	2	8
	15	GAURAV JAYANT FATE		4	3	2	9
	44	YASHI LALITKUMAR PATIL		3	3	2	8
	24	SHANTANU MADHAV KHAIRE		3	2	2	7
9	28	HARSH ULHAS KOSHI	Full Adder	4	3	2	9
	25	PRATHAMESH KHAIRNAR		4	3	2	9
	42	ROSHAN NANDKISHOR PAGAR		4	3	2	9
	54	ADITYA KESHAV RAYATE		4	3	2	9
10	47	PIYUSH YOGESH PATIL	4 bit BCD to Excess 3 code conversion	3	2	2	7
	48	YOGESHWAR JITENDRA PATIL		3	3	2	8
	52	TANMAY PRAMOD PATIL		3	3	2	8
	55	VEDANT HEMANT SAROLKAR		3	3	2	8
11	46	OM ASHOK PATIL	4 bit BCD to Excess 3 code conversion	3	3	2	8
	56	DIKSHANT BHARAT SAWANT		3	3	2	8
12	06	DEEPAK DADASAHEB BHALERAJ	Full Subtractor	4	3	2	9
	10	ROHIT NAMDEV DAHATONDE		4	3	2	9
	17	PRATHAMESH PRAMOD GOSAVI		4	3	2	9
	08	RUTUJA NAMDEO GUNJAL		4	3	2	9
13	27	SHITAL DILIP KHATALE	4 bit BCD to Excess 3 code conversion	4	3	2	9
	19	PRASAD RAMESH NGOLE		4	3	2	9
	36	SAMRUDDHI DEVENDRA MULHERKAR		4	3	2	9
	29	POOJA SUNIL SHIRSAGAR		4	3	2	9

Result Analysis		
Sr. No.		
1	Total Student Present	45
2	Number of Student Scoring above 60%	45

3	Percentage of student Scoring above 60%	100%
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### 9. Impact Analysis:

Questions	3 – Strongly Agree / Excellent	2 – Agree / Good	1- Disagree / Average
Was the Activity Helpful?	35	10	00
Are you able to find application/use of concept covered?	32	13	00
Grade the overall activity?	30	15	00

#### WAS THE ACTIVITY HELPFUL?

Strongly Agree / Excellent
  Agree / Good
  Disagree / Average



#### ARE YOU ABLE TO FIND APPLICATION/USE OF...

Strongly Agree / Excellent
  Agree / Good
  Disagree / Average



#### GRADE THE OVERALL ACTIVITY?

Strongly Agree / Excellent
  Agree / Good
  Disagree / Average



### 10. For review and critique contact: e-mail address of faculty and HOD

1. [suryavanshi.jaya@kbtcoe.org](mailto:suryavanshi.jaya@kbtcoe.org)

2. [hod.it@kbtcoe.org](mailto:hod.it@kbtcoe.org)

Dr. J. R. Suryawanshi

Course In charge

Module Co-coordinator

Dr. V. R. Sonawane

HOD