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II. Contact Details:

a. Office Address:

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III. EDUCATIONAL DETAILS:

Sr. No.	Degree	University	Year of Passing	Class	Percentage
1	Ph. D.	SPPU Pune	Pursuing	–	–
2	M. Tech. (Electronics)	V.J.T.I. Mumbai	2013	Distinction	7.6
3	B. E. (Electronics & Telecommunication)	University of Pune, Pune	2011	First	63.83%
4	HSC	Maharashtra StateBoard	2007	First	64.4 %

IV. EXPERIENCE: Total Teaching Experience: 8 yrs.

Sr. No.	Institution / Organization	Designation	Period	
			From	To
1.	MVP Samaj's Karmaveer Adv. B. G. Thakare College of Engineering, Gangapur Road, Nashik-422013.	Assistant Professor Dept. of E&TC Engineering.	August 1 st , 2013	Till date

V. Number of Seminar, Workshop and Short term Training Programme attended:

COURSE NAME	DURATION	PLACE	TRAINING AGENCY	REMARKS
Control System	2 Week	Nashik	IIT KGP	Completed
Research Methodology	2 Day	Nashik	Department of Computer Engg. MVP KBTCOE Nashik	Completed
LaTeX	2 Day	Nashik	Department of Computer Engg. MVP KBTCOE Nashik	Completed
CMOS Design Using Microwind	2 Day	Nashik	Department of E & TC Engg. MVP KBTCOE Nashik	Completed
ISTE STTP Workshop on CMOS , Mixed-signal ,RF	2 Week	Nashik	IIT KGP	Completed
one-week international faculty development program on "INNOVATIVE TRENDS IN ENGINEERING AND TECHNOLOGY"	1 Week	Online	IQAC, Shree. L. R. Tiwari College of Engineering	Completed
Excel Skills for Business: Intermediate II	4 Week	Online	Coursera	Completed
One Week online Faculty Development Programme on Pedagogical Techniques in Electronics and Electrical Engineering	1 Week	Online	Department of Electronics Engineering, Walchand College of Engineering, Sangli	Completed
One Week Online Short Term Training Program on "VLSI Design Using Cadence Tools: Digital CMOS Design and Verification"	1 Week	Online	Electronics Engineering Department, Sardar Patel Institute of Technology, Andheri(W), Mumbai - 400058	Completed

COURSE NAME	DURATION	PLACE	TRAINING AGENCY	REMARKS
Six days STTP on “VLSI Design Using Cadence Tools: Analog CMOS VLSI Design	1 Week	Online	Electronics Engineering Department, Sardar Patel Institute of Technology, Andheri(W), Mumbai - 400058	Completed
Online Elementary FDP on "Deep Learning and Computer Vision"	1 Week	Online	AICTE Training And Learning (ATAL) Academy	Completed
ACCREDITATION OF UNDERGRADUATE ENGINEERING PROGRAMME	12 Week	Proctored Exam	SWAYAM ONLINE COURSE CERTIFICATION	Completed

VI. Grants Received and Paper Published:

1. Viraj Sonawane, Jagdish Mali, Prof. R N Awale. “DCT Based Image Steganographic Approach”, International Journal of Engineering Research and Applications (IJERA), Vol. 3, Issue 4, Jul-Agu2013, pp. 381-384.
2. Jagdish A. Mali, Viraj Sonawane, Prof. R N Awale., "Image Steganography using Block Level Entropy Thresholding Technique”, International Journal of Engineering Research and Applications (IJERA), Vol. 3, Issue 4, Jul-Aug 2013, pp. 412-415